Application Note
TLIN1431-Q1 Startup Guide

TEXAS INSTRUMENTS

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ABSTRACT

This application note provides an overview of the common bring-up cases of the TLIN1431-Q1 LIN SBC with integrated high-side switch and watchdog. This device can be operated using either of two control modes, determined upon device power-up: pin control or SPI control. In pin control, the device's pins are configured such that the watchdog and state changes of the TLIN1431-Q1 are controlled using logic inputs to the pins. In this control mode, the device is not configurable through SPI. Conversely, in SPI control, the device's pins are configured differently, four of which behave as CLK, SDO, SDI, and nCS, thereby allowing SPI programming for the device. The device operates with a different state diagram between the two control modes, including different triggers for state changes, different state conditions, and different programmability. This report will provide an overview of a general method of powering up the TLIN1431-Q1 into either of these two control modes.

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Trademarks
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1 Startup

The operational control mode of the TLIN1431-Q1 is determined during startup based on the configuration of pin 7 of the device, the PIN/nCS pin. Once the device starts up into either pin control or SPI control, it cannot switch to the other control mode without a power-on reset. Thus, start-up is the most important consideration in determining how the TLIN1431-Q1 behaves.

When the PIN/nCS pin is pulled to GND as shown in Figure 1-1, the device starts up in pin control. See Section 2 for configuration in pin control.
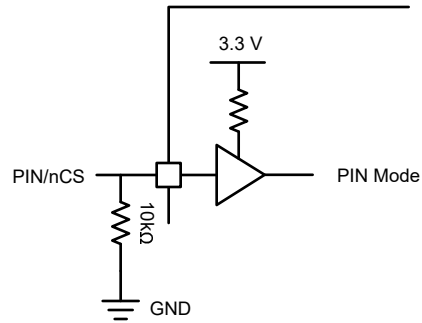
Figure 1-1. PIN/nCS Configuration for Pin Control

When left floating or when pulled to VCC as shown in Figure 1-2, the device operates in SPI control. See Section 3 for a configuration in SPI control, and see Section 1.1 regarding operational voltage selection for the TLIN14315-Q1 (5 V version of the device), which operates without the need for a VIO pin to determine logic-level voltages.
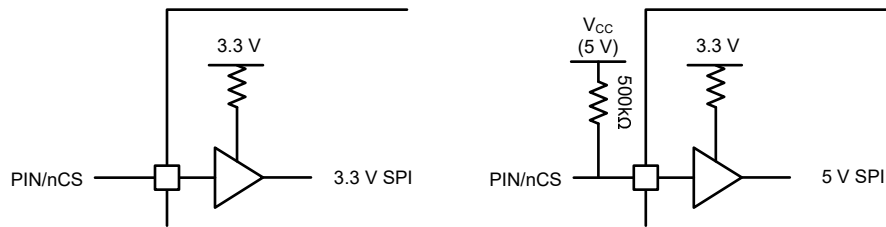
Figure 1-2. PIN/nCS Configurations for SPI Control

1.1 Operational Voltages

The TLIN14313-Q1 (the 3.3 V LDO version of the device) operates using logic level signals of 3.3 V in both pin control and SPI control.

The TLIN14315-Q1 (the 5 V LDO version of the device), is capable of multiple operational voltages without the need for a VIO pin (also known as *VIOless* operation). In SPI control, the connection of the PIN/nCS pin determines whether the device operates using 3.3 V or 5 V SPI communication. As shown in Figure 1-2, leaving the PIN/nCS pin floating causes the device to operate with 3.3 V SPI, while a pull-up to V_{CC} (5 V) results in 5 V SPI operation from the TLIN14315-Q1.

The WKRQ/INH pin can be either a logic-level digital output for wake (WKRQ) or a high-voltage inhibit output (INH) based upon its connection at startup. When externally pulled down by a 100 kΩ resistor, the pin is WKRQ and operates based upon V_{CC}. When left floating or pulled down by a resistor of 1 MΩ or larger, the pin becomes a high-voltage INH output pin. Figure 1-3 shows these two configurations.

Figure 1-3. WKRQ/INH Pin Configurations

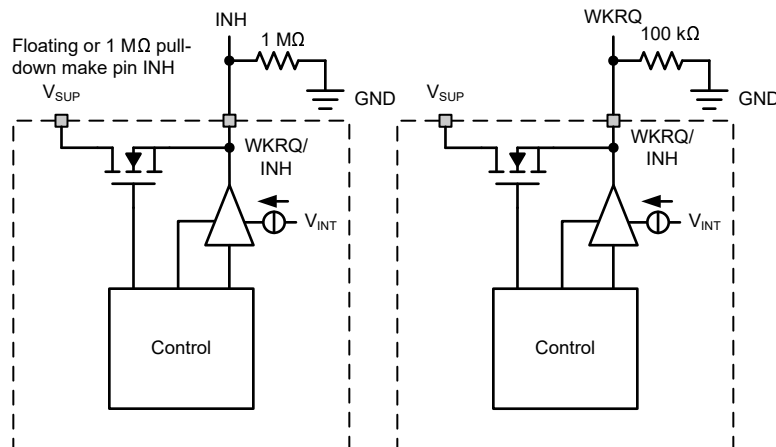It is important for the designer to recognize the behavior and limits of a microprocessor connected to the TLIN1431-Q1 to ensure that necessary design constraints are met. The microprocessor should be able to handle the 5 V I/O signals of the TLIN14315-Q1 if the PIN/nCS pin is pulled up to 5 V, and the WKRQ/INH pin should be properly connected based upon its configuration as either a digital WKRQ signal or a high-voltage INH signal.

1.2 Power-Up and INIT Mode

As the V_{SUP} input is ramping up from off to steady-state, it will pass through two different thresholds of the TLIN1431-Q1. The first is the rising power-on reset threshold (V_{nPORR}), and the second is the rising V_{SUP} under-voltage threshold (UV_{SUPR}). Each of these thresholds enables various circuits in the device to initialize.

After passing the V_{nPORR} threshold, the digital circuitry and internal clocks initialize. Once V_{SUP} exceeds UV_{SUPR}, the LDO begins ramping until it reaches the rising V_{CC} under-voltage threshold (UV_{CC3R} or UV_{CC5R}), at which point the device will enter INIT mode. Figure 1-4 shows a state diagram of the TLIN1431-Q1 during power-up.
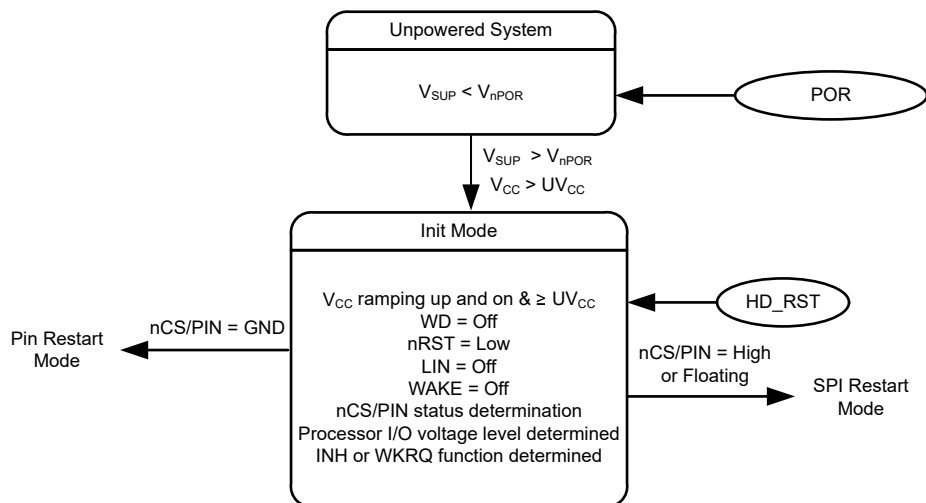
Figure 1-4. INIT Mode State Diagram

Also, during this mode, the device detects the state of the WKRQ/INH pin. During this detection, up to 1.6 V can be seen on the pin as shown in Figure 2-2 and Figure 3-2.

The device exits INIT mode based upon the state of the PIN/nCS pin. Section 2 describes the power-up process in pin control, and Section 3 describes the power-up process in SPI control.

Whenever the device experiences a V_{SUP} drop to a level below UV_{SUPF} (known as V_{SUP} "brownout"), the device will repeat the power-up sequence, shown as "POR" in Figure 1-4. The brownout sequence is shown in Figure 1-5.
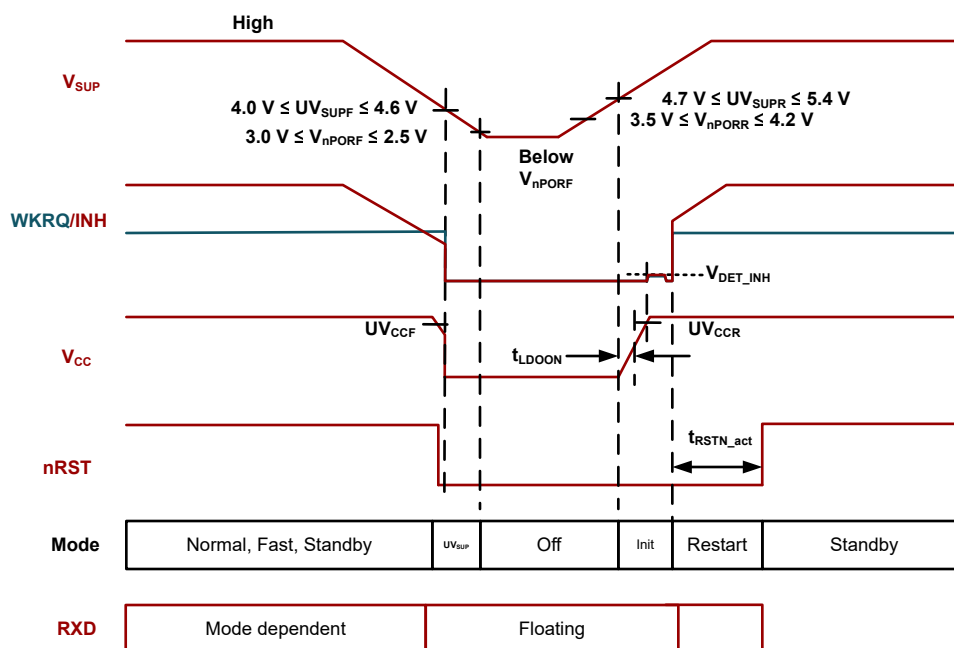
Figure 1-5. Brownout below V$_{nPORF}$

2 Pin Control

In pin control, the device is controlled using the device's I/O pins, and SPI communication is not available.

2.1 Typical Application

Figure 2-1 shows a typical configuration of a TLIN1431-Q1 responder in pin control.
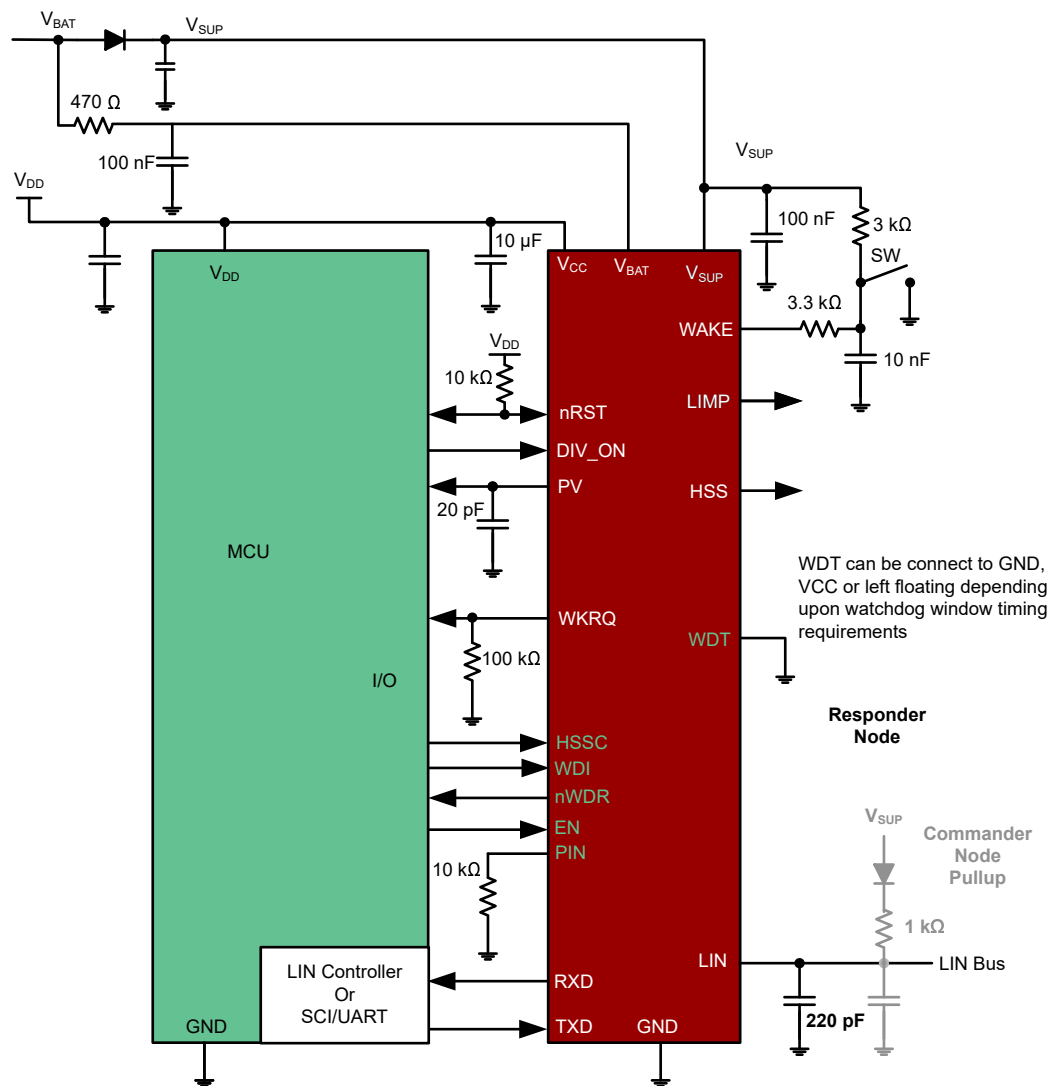
Figure 2-1. Typical Application of TLIN1431-Q1 in Pin Control

Note that PIN is pulled low in this example configuration, resulting in startup in pin control. Also, this application includes a 100 kΩ pull-down resistor on WKRQ/INH, resulting in it behaving as a digital WKRQ pin.

2.2 Power-Up into Normal Mode in Pin Control

Figure 2-2 shows the power-up sequence when starting the TLIN1431-Q1 in pin control, with the PIN/nCS pin pulled to GND with a 10 kΩ resistor.
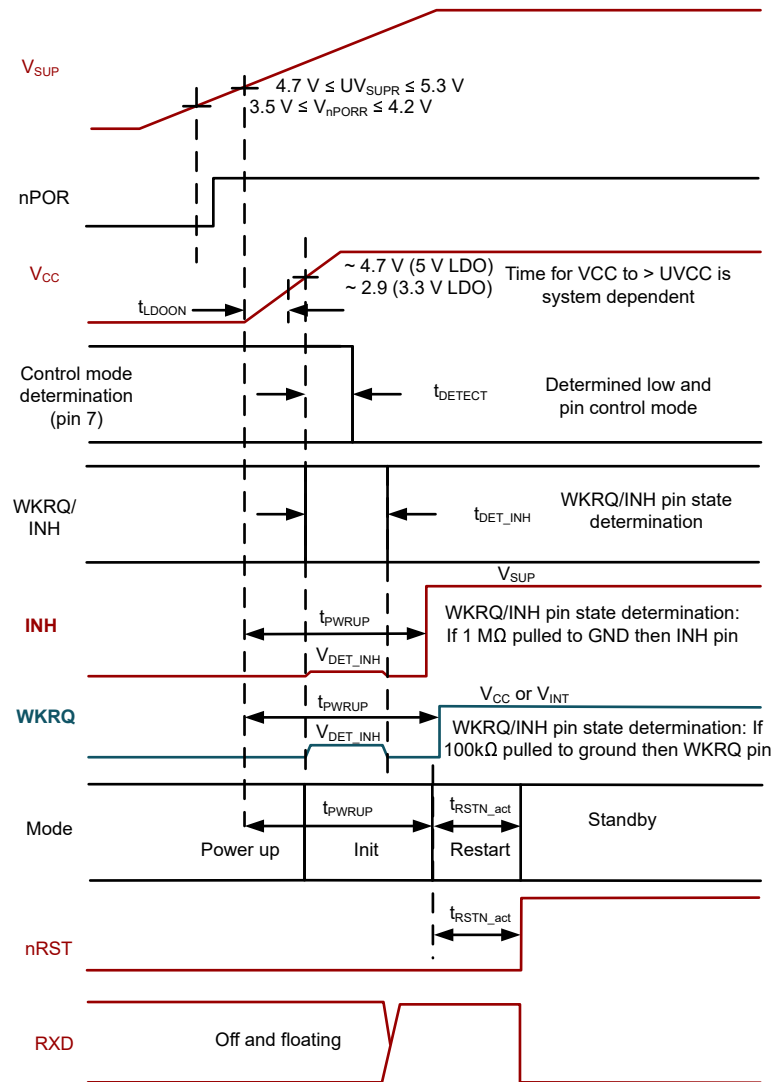
Figure 2-2. Pin Control Power-Up Sequence Timing

To transition to normal mode, the device must first transition from INIT mode through restart mode and standby mode.

2.2.1 Restart Mode from INIT Mode in Pin Control

Restart Mode – Pin Control

WD Failure →

nRST Pulse →

Sleep Mode →

Fail-safe Mode →

V_{CC} = Ramping up (Entrance dependent)
V_{CC} = On (Entrance dependent)
WD = Off
nRST (Power up & Wake event) = Low
nRST (other) = Pulled low for t_{NRST_TOG}
LIN = Off
WAKE = Off
INH or WKRQ = High
LIMP = Same as previous Mode unless WD failure and LIMP is on
HSS = Off

→ Standby Mode

Faults

→ Sleep Mode
SWE timer

→ Fail-safe Mode

Figure 2-3. Restart Mode in Pin Control

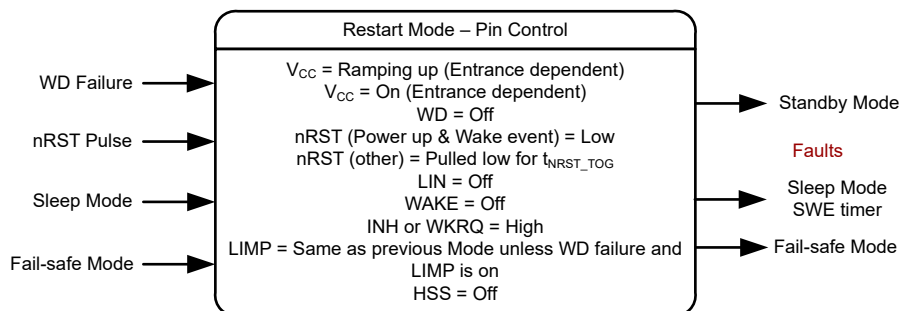During startup, the TLIN1431-Q1 will exit INIT mode into restart mode and will stay in this mode for t_{RSTN_act} before transitioning to standby mode. When entering from sleep mode or fail-safe mode, the SWE timer starts, and the device will transition to sleep mode if this timer expires before entering standby mode. See the device data sheet for more information regarding wake events and fault clearing that must occur in these cases.

2.2.2 Standby Mode from Restart Mode in Pin Control

Standby Mode

← Fast Mode

← Normal Mode

V_{CC} = On
WD = On
nRST = High
LIN = Off
RXD = Indicates a wake event
WAKE = On
INH or WKRQ = High
LIMP = Previous state
HSS = HSSC

← Restart Mode

Faults

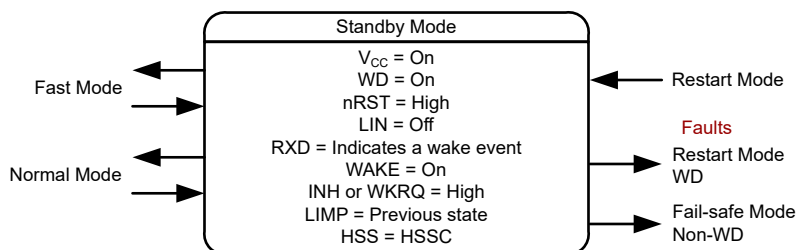→ Restart Mode
WD

→ Fail-safe Mode
Non-WD

Figure 2-4. Standby Mode in Pin Control

In this mode, nRST is released and the device is able to be transitioned to different states. This also starts the watchdog functionality, which must be serviced through a watchdog trigger on WDI within t_{INITWD}. To transition to normal mode, implement this setting:

- EN = high
- TXD = high
- nRST = high for greater than t_{FM_CHANGE}

The device will enter normal mode and data on RXD will be valid after t_{MODE_CHANGE}.

2.2.3 Normal Mode in Pin Control

Normal Mode

Fast Mode →

Standby Mode →

V_{CC} = On
WD = On
nRST = High
LIN = On
WAKE = Off
INH or WKRQ = On
LIMP = Previous state prior to entering
HSS = HSSC

→ Sleep Mode

Faults

→ Restart Mode
WD failure
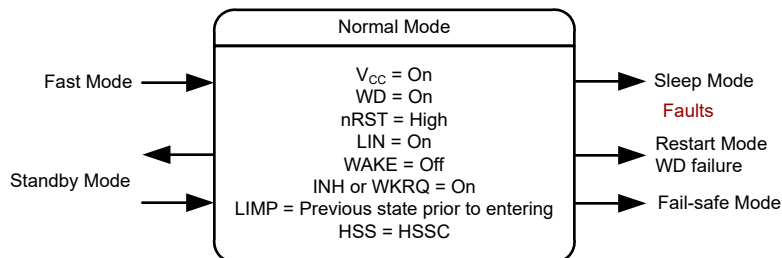
→ Fail-safe Mode

Figure 2-5. Normal Mode in Pin Control

Normal mode is the regular operating state of the TLIN1431-Q1, in which TXD is passed to LIN and LIN is passed to RXD at the LIN-specified maximum of 20 kbps.

From normal mode, the device can transition to sleep more or standby mode. To transition to low-power sleep mode, implement the following configuration for at least t_{EN}:

- EN = low
- TXD = low
- nRST = high

To transition to standby mode, implement the following configuration for at least t_{FM_CHANGE}:

- EN = low
- TXD = high
- nRST = high

In addition, the device will transition to restart mode if a UV_{SUP}, nRST, or watchdog failure event occurs. It will transition to fail-safe mode if a UV_{CC}, OV_{CC}, thermal shutdown, or V_{CC} short-circuit event occurs.
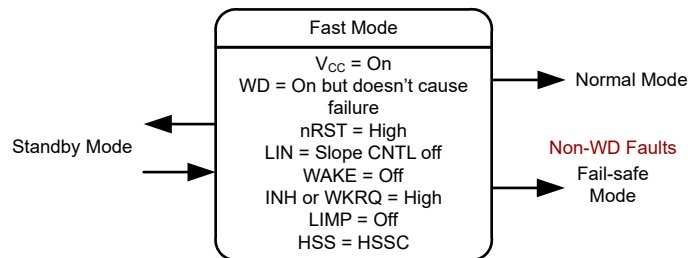
2.3 Power-Up into Fast Mode in Pin Control

Figure 2-6. Fast Mode in Pin Control

Fast mode is a mode designed for end-of-line programming, allowing for data rates up to 200 kbps. To enter fast mode, the same power-up procedure applies as outlined for in Section 2.2 up until the transition out of standby mode. To transition to fast mode from standby mode, implement the same setting as above, but input a low pulse of width t_{FMTXD} on the TXD pin as shown in Figure 2-7. Thus, implement this setting:

- TXD = low pulse for t_{FMTXD} (see Figure 2-7)
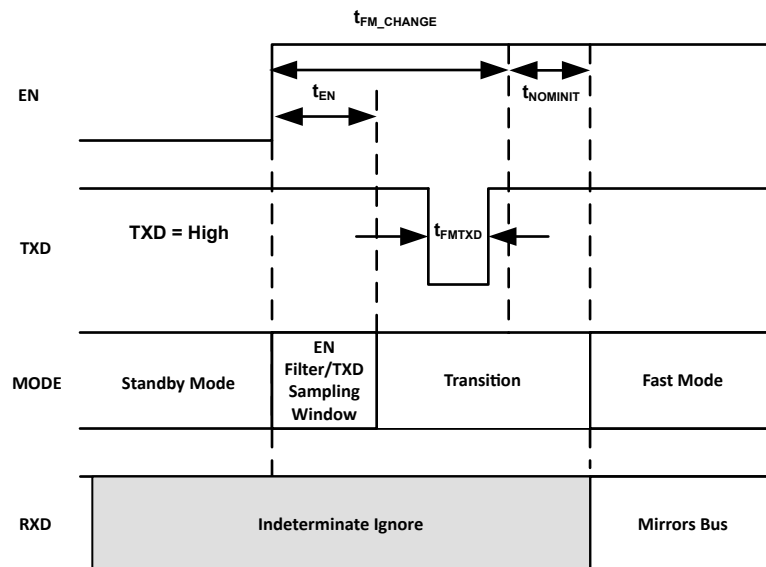- nRST = high
- EN = high for greater than t_{FM_CHANGE}

Figure 2-7. Fast Mode from Standby Mode Sequence Timing in Pin Control

2.4 Sleep Mode to Normal Mode in Pin Control

```
                        ┌─────────────────────────────┐
                        │         Sleep Mode          │
                        ├─────────────────────────────┤
                        │                             │
                        │        V_CC = Off           │
Normal Mode  ──────────▶│        WD: Off              │
                        │        nRST = Low           │
Restart Mode ──────────▶│  LIN = Off but WUP wake able│──────▶ Restart Mode
                        │        WAKE = On            │
Fail-safe Mode ────────▶│   INH or WKRQ = Off         │
                        │        LIMP = Off           │
                        │        HSS = Off            │
                        └─────────────────────────────┘
```
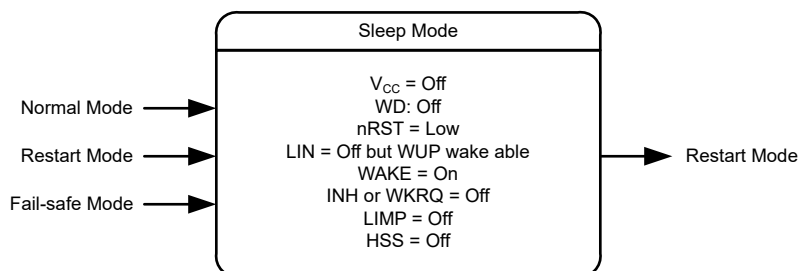
Figure 2-8. Sleep Mode in Pin Control

To return to normal mode from sleep mode, the device must first transition to restart mode due to one of the following conditions:

- LIN bus wake-up
- WAKE pin state change
- EN = high for greater than t_{FM_CHANGE}

Once the device transitions to restart mode, the SWE timer starts. The device must enter standby before this timer times out. Additionally, all faults must be cleared from the device. If either of these two conditions are not met, the device re-enters sleep mode. Otherwise, the same procedure outlined in Section 2.2.2 and Section 2.2.3 applies.
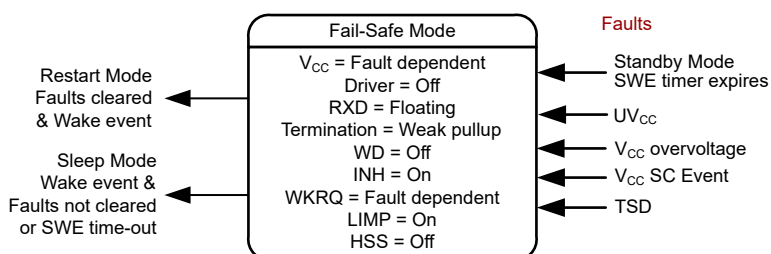
2.5 Fail-Safe Mode to Normal Mode in Pin Control

```
                                      ┌──────────────────────────────┐           Faults
                                      │        Fail-Safe Mode        │
                                      ├──────────────────────────────┤◀── Standby Mode
Restart Mode                          │   V_CC = Fault dependent     │      SWE timer expires
Faults cleared  ◀────────────────────│        Driver = Off          │
& Wake event                          │        RXD = Floating        │◀── UV_CC
                                      │   Termination = Weak pullup  │
Sleep Mode                            │        WD = Off              │◀── V_CC overvoltage
Wake event &    ◀────────────────────│        INH = On              │◀── V_CC SC Event
Faults not cleared                    │   WKRQ = Fault dependent     │
or SWE time-out                       │        LIMP = On             │◀── TSD
                                      │        HSS = Off             │
                                      └──────────────────────────────┘
```

Figure 2-9. Fail-Safe Mode in Pin Control

The device enters fail-safe mode if any of these events occur:

- UV_{CC} (V_{CC} undervoltage)
- OV_{CC} (V_{CC} overvoltage)
- TSD (thermal shutdown)
- V_{CCSC} (V_{CC} short-circuit)

To successfully transition from fail-safe mode to normal mode, all of these faults must be cleared. Exiting this mode requires a wake event to take place, which transitions the device to restart mode. If faults are cleared, transition to normal mode can take place as described in Section 2.2.2 and Section 2.2.3. If faults are not cleared, the device will enter sleep mode after the SWE timer expires.

3 SPI Control

In SPI control, the device is controlled through SPI communication using pins 4 through 7 (CLK, SDO, SDI, and nCS).

3.1 Typical Application

Figure 3-1 shows a typical configuration of a TLIN1431-Q1 responder in SPI control.
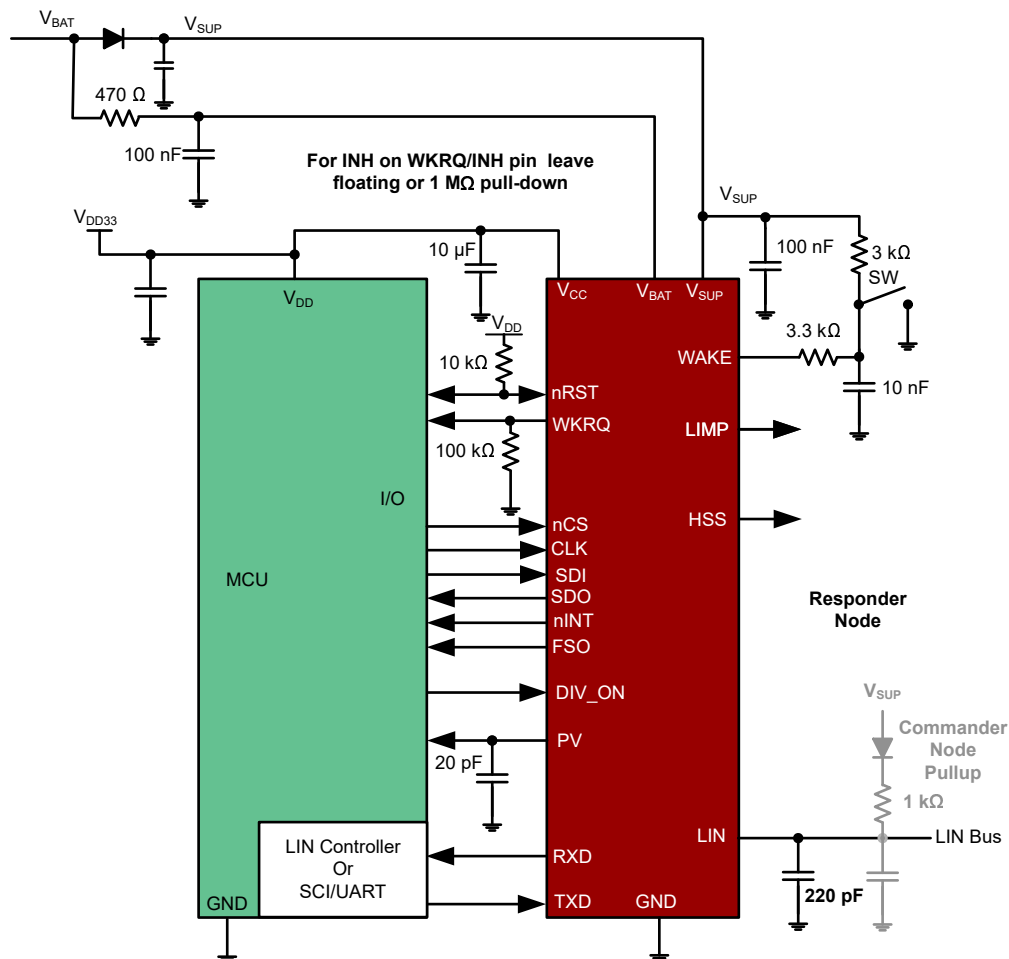

Figure 3-1. Typical Application of TLIN1431-Q1 in SPI Control

Note that PIN/nCS is *not* pulled low in this example configuration. When the TLIN1431-Q1 sees a high-impedance to this pin at startup, the device enters SPI control. Also, this application includes a 100 kΩ pull-down resistor on WKRQ/INH, resulting in it behaving as a digital WKRQ pin.

3.2 Power-Up into Normal Mode in SPI Control

Figure 3-2 shows the power-up sequence when starting the TLIN1431-Q1 in SPI control, with the PIN/nCS pin either high-impedance or pulled high to V_{CC}.
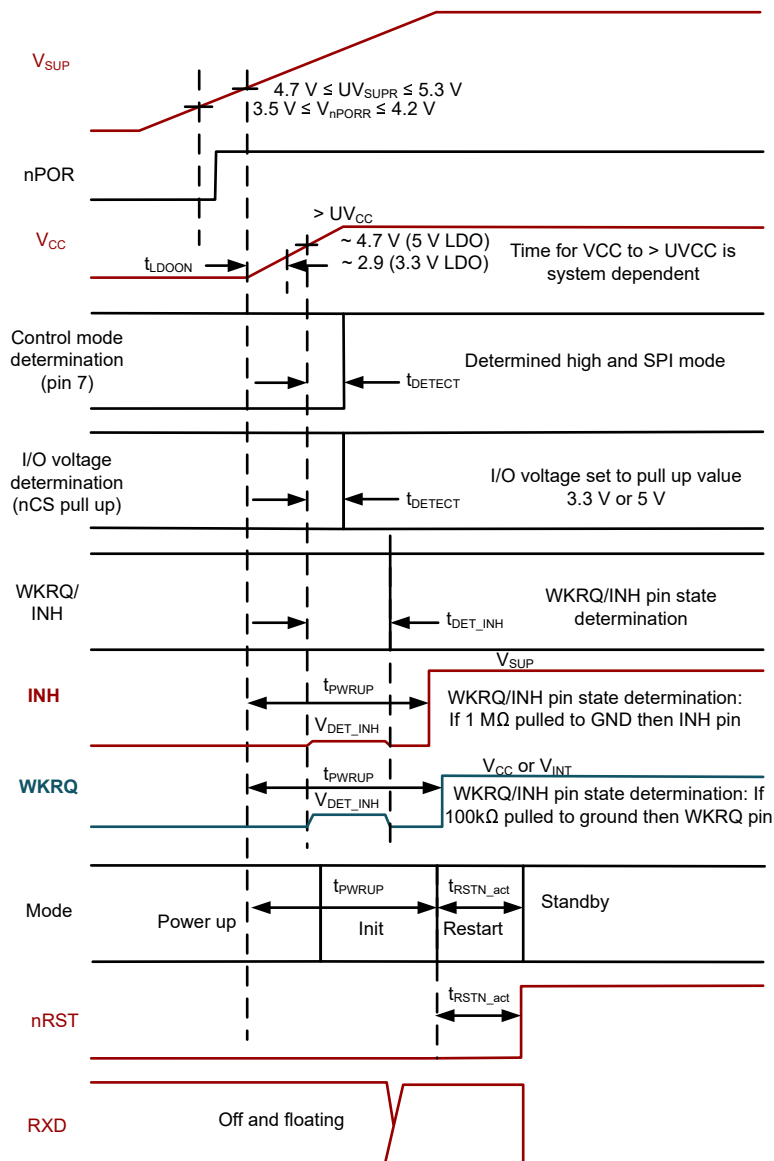
Figure 3-2. SPI Control Power-Up Sequence Timing

To transition to normal mode, the device must first transition from INIT mode through restart mode and standby mode.
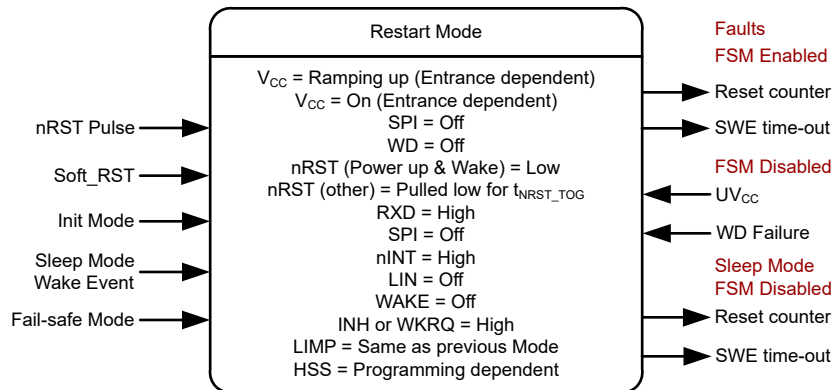
3.2.1 Restart Mode from INIT Mode in SPI Control

Figure 3-3. Restart Mode in SPI Control

During startup, the TLIN1431-Q1 will exit INIT mode into restart mode and will stay in this mode for t_{RSTN_act} before transitioning to standby mode. Each time the device enters restart mode, the restart counter is incremented. This should be regularly cleared to prevent the device from entering fail-safe mode due to too many restarts. See the device data sheet for more information regarding RSRT_CNTR (8'h28).

3.2.2 Standby Mode from Restart Mode in SPI Control
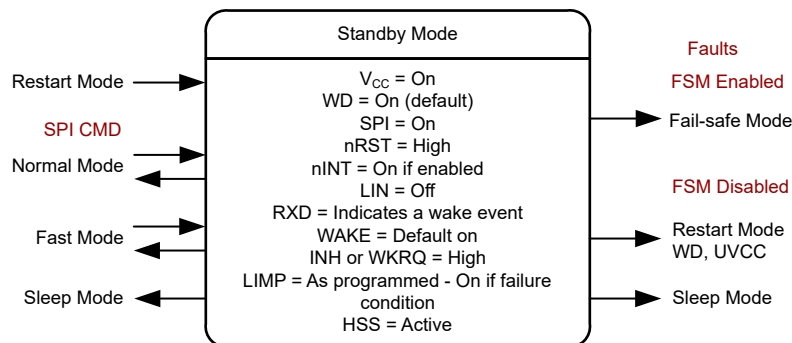
Figure 3-4. Standby Mode in SPI Control

In this mode, nRST is released and the device is able to be transitioned to different states. This also starts the watchdog functionality, which must be serviced through a watchdog trigger on WDI within t_{INITWD}. To transition to normal mode, use the LIN_CNTRL register by setting 8'h1D[7:6] (LIN_MODE) to 10b. The device will enter normal mode and data on RXD will be valid after t_{MODE_CHANGE}.

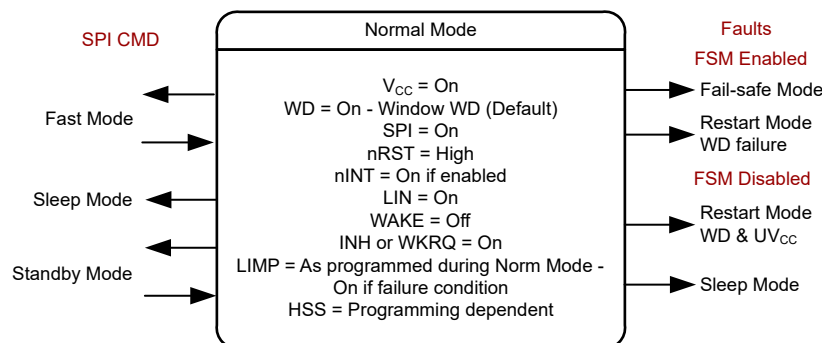### 3.2.3 Normal Mode in SPI Control

Figure 3-5. Normal Mode in SPI Control

Normal mode is the regular operating state of the TLIN1431-Q1, in which TXD is passed to LIN and LIN is passed to RXD at the LIN-specified maximum of 20 kbps.

From normal mode, the device can be transitioned to any of the following states through a SPI command, setting the LIN_MODE bits of the LIN_CNTRL register (8'h1D[7:6]) to any of the following values:

- 00b = Standby mode
- 01b = Sleep mode
- 10b = Normal mode (current mode)
- 11b = Fast mode

In addition, the device will transition to restart mode if a UV_{SUP}, nRST, watchdog failure, or SOFT_RST event occurs. It will transition to fail-safe mode (if enabled) or sleep mode (if FSM disabled) if a UV_{CC}, OV_{CC}, thermal shutdown, or V_{CC} short-circuit event occurs.

3.3 Power-Up into Fast Mode in SPI Control
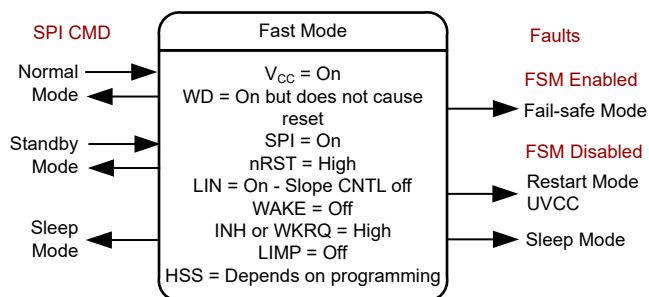
Figure 3-6. Fast Mode in SPI Control

Fast mode is a mode designed for end-of-line programming, allowing for data rates up to 200 kbps. To enter fast mode, the same power-up procedure applies as outlined for in Section 3.2 up until the transition out of standby mode. To transition to fast mode from standby mode, set the LIN_MODE bits of the LIN_CNTRL register (8'h1D[7:6]) to 11b.

The device can also transition into fast mode from normal mode using the same SPI command.

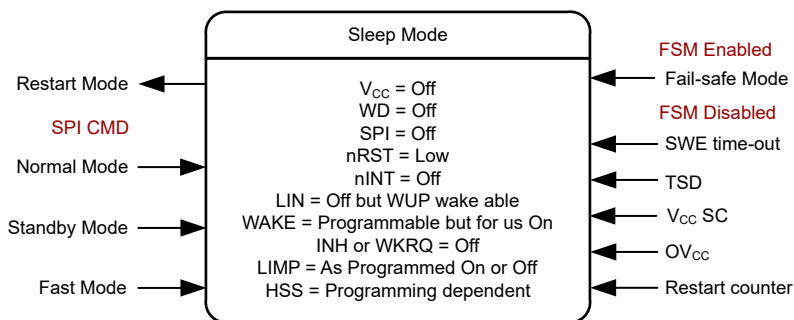## 3.4 Sleep Mode to Normal Mode in SPI Control

Figure 3-7. Sleep Mode in SPI Control

Sleep mode can be accessed from normal mode, standby mode, or fast mode through a SPI write by setting the LIN_MODE bits of the LIN_CNTRL register (8'h1D[7:6]) to 01b.

To return to normal mode from sleep mode, the device must first transition to restart mode due to one of the following conditions:

- LIN bus wake-up
- WAKE pin state change

Once the device transitions to restart mode, the SWE timer starts. The device must enter standby before this timer times out. Additionally, all faults must be cleared from the device. If either of these two conditions are not met, the device re-enters sleep mode. Otherwise, the same procedure outlined in Section 3.2.2 and Section 3.2.3 applies.

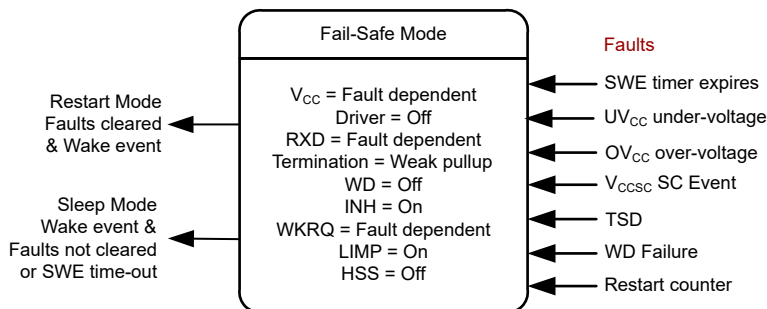## 3.5 Fail-Safe Mode to Normal Mode in SPI Control

Figure 3-8. Fail-Safe Mode in SPI Control

Fail-safe mode can be disabled through a SPI write by setting the FSM_DIS bit of the FSM_CONFIG register (8'h17[0]) to 1b. If fail-safe mode is enabled, the device enters fail-safe mode if any of these events occur:

- UV_{CC} (V_{CC} undervoltage)
- OV_{CC} (V_{CC} overvoltage)
- TSD (thermal shutdown)
- V_{CCSC} (V_{CC} short-circuit)
- SWE timeout in standby mode

To successfully transition from fail-safe mode to normal mode, all of these faults must be cleared. Exiting this mode requires a wake event to take place, which transitions the device to restart mode. If faults are cleared, transition to normal mode can take place as described in Section 3.2.2 and Section 3.2.3. If faults are not cleared, the device will enter sleep mode after the SWE timer expires.

Each time the device enters fail-safe mode, the fail-safe mode counter is incremented. This counter (8'h18[3:0]) should be regularly set to 0 by a SPI command. Otherwise, if the counter reaches the limit (set in 8'h18[7:4]), then the action prescribed in FSM_CNTR_ACT (8'h17[7:4]) will take place.

Additionally, FS_STAT (8'h17[3:1]) provides the reason the device entered fail-safe mode, and SWE_TIMER_SET (8'h1C[6:3]) sets the length of time the SWE timer can support, ranging from 30 seconds to 10 minutes (defaulted to 5 minutes).

3.6 Configuring Watchdog through SPI

The watchdog function has extensive configurability, including selecting the watchdog mode, timeout window, and activation. By default, watchdog is enabled in standby mode, but it can be disabled by setting WD_STBY_DIS (8'h14[0]) to 1b. It can be disabled altogether by setting WD_CONFIG (8'h13[7:6]) to 00b.

Each time a watchdog error occurs, the watchdog error counter is incremented, accessible through WD_ERR_CNT (8'14[4:1]). When this counter reaches the maximum value per WD_ERR_CNT_SET (8'h16[7:6]), the device transitions to restart mode, the error counter is reset back to one, and nRST is pulled low for t_{NRST_TOG}.

Pin Assignments in Pin Control vs. SPI Control

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4 Pin Assignments in Pin Control vs. SPI Control

The TLIN1431-Q1 is capable of operating in one of two different configurations: pin control or SPI control. Pins 4 through 9 of the device change functionality based upon this configuration, as shown in Table 4-1.

Table 4-1. Functional Differences Between Pins 4 through 7 in Pin Control vs. in SPI Control

Pin	Pin Control	SPI Control
4	**WDT** – Programmable watchdog window set input	**CLK** – SPI clock input
5	**nWDR** – Watchdog failure output trigger	**SDO** – SPI serial data output
6	**WDI** – Watchdog timer edge-triggered input	**SDI** – SPI serial data input
7	**PIN** – Input that sets the device to pin control	**nCS** – SPI chip select
8	**EN** – Device mode change input	**nINT** – Device interrupt output
9	**HSSC** – High-side switch control input	**FSO** – Function output

In pin control, the device's watchdog and state changes are controlled by the device's pins, and SPI communication is not available. In SPI control, the device's watchdog and state changes are controlled by SPI communication.

Once the device has started up into either pin control or SPI control, it is not possible for the device to change control modes without a power-on reset. Consequently, each time a power-on reset occurs, the state of pin 7 determines whether the device starts up into pin control or SPI control.

5 References

- Texas Instruments, TLIN1431-Q1 Automotive LIN SBC with Integrated High-Side Switch and Watchdog data sheet.